Quantized Conduction and High Mobility in Selectively Grown $In_xGa_{1-x}As$ Nanowires

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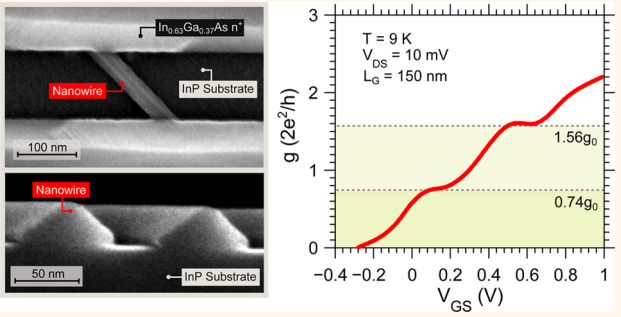
ABSTRACT We report measured quantized conductance and quasi-ballistic transport in selectively regrown $In_{0.85}Ga_{0.15}As$ nanowires. Very low parasitic resistances obtained by regrowth techniques allow us to probe the near-intrinsic electrical properties, and we observe several quantized conductance steps at 10 K. We extract a mean free path of 180 ± 40 nm and an effective electron mobility of 3300 ± 300 $cm^2/V \cdot s$, both at room temperature, which are among the largest reported values for nanowires of similar dimensions. In addition, optical characterization of the nanowires by photoluminescence and Raman measurement is performed. We find an unintentional increase of indium in the $In_xGa_{1-x}As$ composition relative to the regrown film layer, as well as partial strain relaxation.



KEYWORDS: field-effect transistors · nanowire · electric transport · mobility · InGaAs · ballistic transport · selective regrowth · photoluminescence · Raman

Indium-rich $In_xGa_{1-x}As$ nanowires have gathered much research attention recently due to their excellent electron transport properties.[1] In particular, InAs nanowires have been shown to have a mobility at least an order of magnitude higher than that of silicon nanowires.[2,3] Moreover, the ease by which ohmic contacts are formed into $In_xGa_{1-x}As$ and the possibility of low-defect high-k oxide interfaces have made $In_xGa_{1-x}As$ one of the primary considerations as the replacement for silicon channels in n-type metal-oxide-semiconductor field-effect transistors (MOSFETs).[4−7] The implementation of III−V MOSFETs, such as $In_xGa_{1-x}As$, will likely be in the form of 1D nanowires with diameters less than 30 nm.[8] The use of nanowires as the channel in MOSFETs offers enhanced performance compared to traditional planar channels, through improved electrostatic control. The combination of high-mobility materials and short gate lengths (~30 nm) of state-of-the-art MOSFETs indicates operation in the ballistic or quasi-ballistic regime. Together with 1D channels, such devices display unique characteristics, notably quantized conduction and step-like features in the conductance at low temperatures.

Several methods of fabricating $In_xGa_{1-x}As$ nanowires have been reported. In particular, nanowires grown by the vapor−liquid−solid (VLS) technique, employing a metal particle catalyst, have been widely studied.[9] VLS-grown InAs nanowires, for instance, exhibit mobility ranging from 2000 to 5000 $cm^2/V \cdot s$ at nanowire diameters of <30 nm.[10] Etched-out $In_{0.70}Ga_{0.3}As$ nanowires have also recently been studied.[11] However, due to increased surface scattering, the mobility of nanowires with a diameter <30 nm is typically more than 2 orders of magnitude lower than bulk mobility.[10] For this reason, the preservation of high-quality nanowire side-walls must be a high priority.[12,13] In this work, we electrically and optically characterize selectively grown InGaAs nanowires that are parallel to the surface. We fabricate MOSFET test devices with very low parasitic resistances using a contact regrowth technique, allowing us to probe the near-intrinsic electrical transport properties of the nanowires. Multiple quantized conductance steps are

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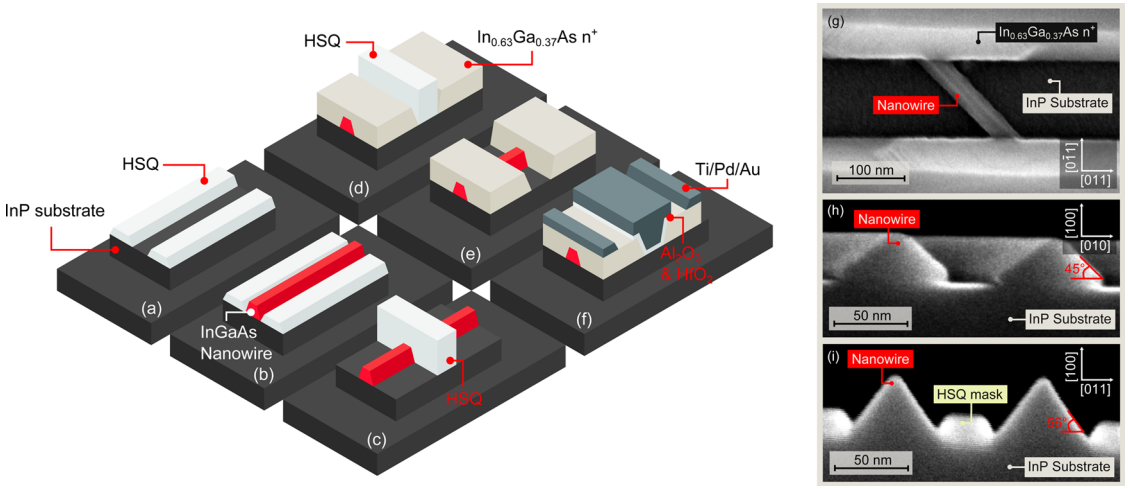

Figure 1. (a) HSQ is patterned on InP/Fe semi-insulating substrate using EBL. (b) $In_{0.63}Ga_{0.37}As$ is regrown by MOCVD using the HSQ as a growth mask. A nanowire is formed between the HSQ-covered areas. (c) HSQ is stripped by buffered oxide etch (BOE), and another HSQ film is applied and patterned as a thin line across the nanowire. (d) Highly doped $In_{0.63}Ga_{0.37}As$ is regrown by MOCVD. (e) HSQ is stripped by BOE. The highly doped regions on each side of the nanowire constitute the source and drain of the MOSFET. (f) Al_2O_3 and HfO_2 are deposited by atomic layer deposition (10 and 60 cycles, respectively). Metallization is performed by lift-off. (g) SEM image of the device corresponding to stage (e). (h,i) Cross-sectional SEM images of wider reference nanowires in two different directions.

observed at $T_L = 10$ K. We explain the characteristics by use of the ballistic MOSFET theory.[14] The extracted electron mobility obtained from the mean free path at room temperature is 3300 ± 300 $cm^2/V \cdot s$, among the highest reported for nanowires of any material system. Optical characterization reveals increased indium levels in the nanowires as well as partial strain relaxation as compared with planar film growth. These results show the potential of selectively grown lateral InGaAs nanowires for high-performance MOSFET devices. We would also like to highlight the potential use of nanowires with a long mean free path in the search for Majorana Fermions.[15]

METHODS

Figure 1a–f shows schematics of the fabrication process of the test device.[16] First, hydrogen silsesquioxane (HSQ) is patterned by electron beam lithography (EBL) on semi-insulating (100) InP/Fe. HSQ is transformed to SiO_2 when cured by electron beam exposure. This enables it to act as a growth mask during the subsequent metal–organic chemical vapor deposition (MOCVD) growth of 15 nm $In_{0.63}Ga_{0.37}As$, resulting in a nanowire composition of $In_{0.85}Ga_{0.15}As$ as obtained from optical characterization. Parallel to the surface, a nanowire is formed in the narrow space between HSQ-covered areas. Figure 1g shows a scanning electron microscopy (SEM) image of a single-nanowire device. Figure 1h,i shows cross-sectional SEM images of wider reference nanowires oriented with their length along the [001] and [011] directions, respectively. From the facet angles, we deduce that [001] nanowires are defined by {110} facets and [011] nanowires by {111}B facets. In order to obtain optimal facets of the subsequent contact regrowth layer, the fabricated devices utilize nanowires oriented along [001].

The dimensions of the nanowire are further scaled down by several cycles of digital etching through ozone oxidation and diluted HCl etching.[17] The root mean square surface roughness of the top nanowire surface is determined from atomic force microscopy measurements as <0.4 nm, below or at the resolution limit of the measurement system (Supporting Information). The final width and height of the nanowire are 28 and 10 nm, respectively. Subsequently, an HSQ line, which serves to define the gate length, L_G, of the device, is patterned across the nanowire, and a second MOCVD regrowth step of 40 nm $In_{0.63}Ga_{0.37}As$ n^{++} ($N_D = 5 \times 10^{19}$ cm^{-3}) is performed. The highly doped regions form the source and drain of the device and facilitate low contact resistances. Prior to atomic layer deposition of the gate oxide (10 cycles Al_2O_3 and 60 cycles HfO_2), the nanowires are passivated by sulfur treatment. Subsequently, gate metal (Ti/Pd/Au) is evaporated and deposited by lift-off. The gate oxide is then removed in the source and drain regions, using the gate metal as the mask, but remains under the gate metal overlap with source and drain as isolation. Ti/Pd/Au contact metal is deposited by lift-off of 600 nm from each side of the gate metal. Au pad metallization by lift-off finalizes the process.

RESULTS AND DISCUSSION

The conductance $g = dI_{DS}/dV_{DS}$ of a representative device is shown in Figure 2a. Two distinct step-like features, corresponding to two sub-band levels, are observed at $g_1 = 0.74g_0$ and $g_2 = 1.56g_0$, where $g_0 = 2q^2/h$. From the Landauer–Büttiker formalism, each sub-band is expected to increase the device

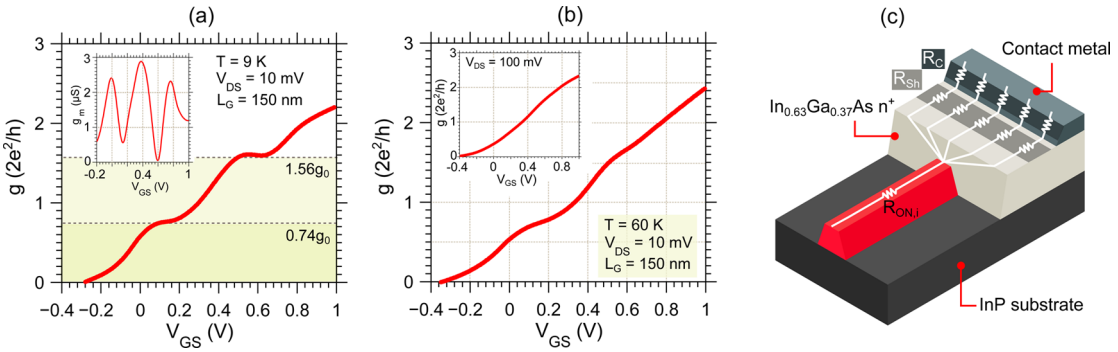

Figure 2. (a) Conductance $g = dI_{DS}/dV_{DS}$ *versus* V_{GS} of an InGaAs nanowire MOSFET at 10 K. Inset shows the transconductance $g_m = dI_{DS}/dV_{GS}$ for the same device and conditions. (b) $g-V_{GS}$ for the same device at 60 K. Inset shows $g-V_{GS}$ at large V_{DS}. (c) Schematic figure of the resistances in a device from the drain or source side. The total on-resistance is constituted by the intrinsic on-resistance of the nanowire, $R_{ON,i}$, and a parasitic resistance, R_P, which is a spreading access resistance constituted by the contact resistance, R_C, and the sheet resistance, R_{Sh}.

conductance by $g = Tg_0$, where T is the transmission. For fully ballistic transport, $T = 1$. We note that g_2 is approximately twice the level of g_1, which indicates that the transmission to each sub-band is similar. The further increased I_{DS} beyond g_2 is sign of a third sub-band level within the V_{GS} measurement range, which is also revealed by a third g_m peak in the inset. I_{DS} at higher V_{GS} was not measured due to the risk of device breakdown. Generally, the number of conductance steps visible in a given V_{GS} measurement range is determined by several factors: (i) The nanowire dimensions set the band structure, that is, the energy separation between sub-bands. (ii) L_G together with (iii) the mean free path determine the transmission. (iv) The gate capacitance and (v) the oxide interface trap density (D_{it}) determine the control of V_{GS} on the band structure in the nanowire. For example, high gate capacitance and low D_{it} will reduce the V_{GS} separation between conductance steps, allowing for more visible steps in a given V_{GS} range. At 60 K, the step-like features are much less distinct, as shown in Figure 2b. At V_{DS} = 100 mV, the steps are not visible (inset). Except for thermal broadening, we observe no apparent dependence of g_1 or g_2 on temperature, which implies that the dominant scattering mechanism is temperature-independent surface roughness scattering.[18] The steps are visible up to 120 K (see Supporting Information). Similarly, the device transconductance $g_m = dI_{DS}/V_{GS}$ is ideally 0 unless V_{GS} causes a sub-band to enter the conducting window, forming peaks at those energies. The conductance steps become less visible as eV_{DS} nears the energy separation between sub-bands or the sub-bands are sufficiently thermally broadened.

The mean free path of a single nanowire λ_s is determined from the transmission $T = \lambda_s/(\lambda_s + L_G)$, with the conductance for the first sub-band being $g_1 = Tg_0 \approx 0.74g_0$ and L_G = 150 nm. Thus, we obtain $\lambda_s = 350 \pm 50$ nm for the first sub-band of a single device. The error margins are due to uncertainty in determining the exact value of T for the conductance step. A similar value was reported by Chuang *et al.*[18] for a single VLS-grown nanowire with d = 26 nm: $T \approx 80\%$ at L_G = 60 nm, corresponding to a peak $\lambda_s = 280 \pm 50$ nm, and an average $\lambda = 150 \pm 40$ nm is extracted from the L_G dependence.

To obtain an accurate value of λ_s, the parasitic resistances of the device must be calculated. Figure 2c shows a schematic of the resistances from the source or drain side in a device. The total on-state resistance of a device is $R_{ON} = R_{ON,i} + R_P$, where $R_{ON,i}$ is the intrinsic on-resistance and R_P is the parasitic spreading access resistance which comes from R_C and R_{Sh}. $R_C = 25\ \Omega\cdot\mu$m is the contact resistance due to the ohmic metal contacts to the n^+ $In_{0.63}Ga_{0.37}As$ layer, extracted from on-sample transmission line method measurements. R_{Sh} is a contribution from the sheet resistance ($R_\square = 70\ \Omega/\square$) of the n^+ $In_{0.63}Ga_{0.37}As$ layer through the ~100 nm distance between the contact metal and the nanowire. Using the measured values of R_C and R_{Sh}, we calculate the spreading access resistance $R_P = 150 \pm 50\ \Omega$ by COMSOL 3D simulation. This includes the resistance added from a possible Schottky barrier between the metal contact and the n^+ $In_{0.63}Ga_{0.37}As$ layer. This resistance is negligible compared to $1/g_0$ = 12.9 kΩ, which means that the calculation of λ_s from T is accurate.

To determine the average room temperature λ of our nanowires, we fabricated devices with 100 parallel nanowires and L_G from 50 to 225 nm (a total of 20 devices). Figure 3a shows an SEM image of such a device. Conductance steps are not visible in these devices due to the many parallel nanowires with slight width variations (±2 nm). To obtain λ, we use the resistance of a ballistic MOSFET in the on-state, described as

$$R_{ON} = \frac{h}{2q^2M\lambda}L_G + \frac{h}{2q^2M} + R_P$$

where R_P is the total parasitic resistance and M is the number of conducting sub-bands.[19] R_{ON} per nanowire for these devices is shown in Figure 3b. Due to the tightly packed parallel nanowires, R_P is larger than that

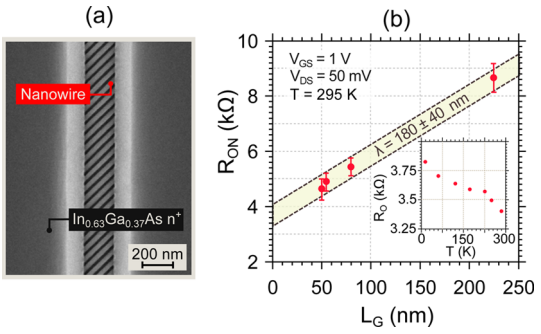

Figure 3. (a) SEM image of the MOSFET device with 100 parallel nanowires. (b) On-resistance per nanowire *versus* gate length for the same type of devices at room temperature. Inset shows on-resistance *versus* temperature for a single device with L_G = 50 nm.

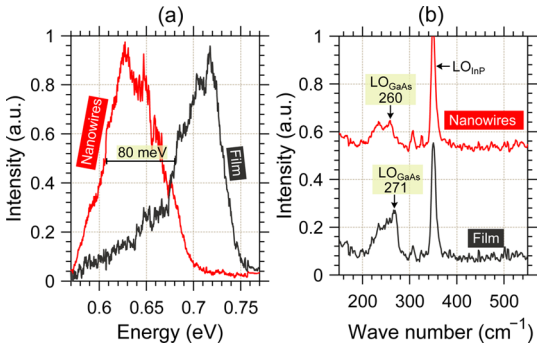

Figure 4. (a) Photoluminescence measurements for nanowires and $In_{0.53}Ga_{0.47}As$ film on the same sample. Band gap narrowing due to background doping is 80 meV. (b) Raman spectroscopy results for the same nanowires and film.

in the single-nanowire device. Source and drain contacts each add $R_C \approx 800\ \Omega$ and $R_{Sh} \approx 100\ \Omega$ per nanowire. Furthermore, the width of the highly doped contact region is approximately twice that of the total width of the nanowires, so the total parasitic resistance is $R_P = R_C \approx 800\ \Omega$, which can be compared to $R_{ON} \approx 4\ k\Omega$ at L_G = 50 nm. Using this value, we obtain an average $\lambda = 180 \pm 40$ nm at room temperature. The error margin comes from the spread in R_{ON} for devices at the same L_G, which may be due to several causes, such as nanowire width variations, contact resistance variations, and nanowire defects. This value of λ overlaps those reported for the VLS-grown vertical nanowires and compares favorably to those reported for etch-defined lateral nanowires.[18] For instance, Thathachary *et al.*[11] showed λ = 100 nm for W_{NW}/H_{NW} = 40/10 nm etch-defined lateral nanowires at room temperature utilizing gated Hall measurements.

The room temperature near-equilibrium electron field-effect mobility of our nanowires is $\mu_e = 3300 \pm 300\ cm^2/V\cdot s$, calculated from[19]

$$\mu_e = \frac{C_F q \lambda v_T}{2kT_L}$$

which comes from $D_n = \lambda V_T/2$ and the Einstein relation utilizing a correction factor $C_F = 2.75 \pm 0.25$, which comes from the degenerate conditions. We use $E_F - E_C = 87.5 \pm 12.5$ meV in our calculations, corresponding to 3−4 filled sub-bands. We note that this method of calculating the mobility from the mean free path is not influenced by D_{it} because D_{it} does not directly impact the transmission of each sub-band. Generally, D_{it} can have a significant impact on the extracted field-effect mobility in III−V field-effect transistors. This value of the electron mobility is close to the other reported values in $In_xGa_{1-x}As$ nanowires with similar dimensions formed by VLS growth.[20−24] For instance, Ford *et al.* reported VLS-grown InAs nanowires with a field-effect mobility of 1000−7000 $cm^2/V\cdot s$ for diameters of d = 10−40 nm.[10] For silicon nanowires, Kotlyar *et al.*[12] determined a field-effect mobility of 100−250 $cm^2/V\cdot s$ for d = 10−25 nm from simulations. The relatively high mobility in our nanowires may be due to a lack of stacking faults orthogonal to the current (as has been reported for VLS-grown nanowires[25]) and high-quality side-wall surfaces.

From R_{ON} in Figure 3b, we are also able to extract M using the estimated value of R_P. We obtain $M = 3.5 \pm 0.5$, which is in agreement with the value observed in the conductance plot, M = 3 at 10 K. We observe a slight increase of R_{ON} as T_L is lowered, as shown in the inset of Figure 3b for an L_G = 50 nm device. This may be due to a nonideal metal/semiconductor junction, forming a small Schottky barrier.

The composition and strain of the nanowires were characterized by photoluminescence (PL) and Raman spectroscopy. To obtain strong signals, we prepared samples with 20 μm × 10 μm areas covered with large reference nanowires (the cross section of which is seen in Figure 1h), well below the spot size of the laser. The dimensions of these nanowires are W/H = 50/30 nm. Two samples were prepared with $In_{0.53}Ga_{0.47}As$ and $In_{0.63}Ga_{0.37}As$ nominal epitaxial growth, respectively. The composition of the 2D layer outside of the nanowire area was confirmed by X-ray diffraction measurements to coincide with the nominal growth. Figure 4a shows the result of the PL measurement at 10 K using a 532 nm laser for the $In_{0.53}Ga_{0.47}As$ sample. The InGaAs peak of the nanowires is red-shifted by approximately 80 meV relative the $In_{0.53}Ga_{0.47}As$ film peak, which was measured outside the nanowire-covered area on the same sample. The background doping of the film layer was obtained from Hall measurements as $N_D \approx 5 \times 10^{17}\ cm^{-3}$. This causes band gap narrowing of approximately 80 meV, which we assume is identical for the nanowires. Using a 2D self-consistent effective mass Schrödinger−Poisson solver, we estimate that the nanowire size quantization increases the band gap by 15 meV, which is not accounted for in these calculations. This will cause a small underestimation of the calculated indium content and strain. The peak shift cannot directly be translated to a composition shift because any composition shift from $In_{0.53}Ga_{0.47}As$

will result in strain due to lattice mismatch to the InP substrate.[26] For instance, an increase of the indium composition can result in a maximum compressive strain up to 3.8% for InAs, which would cause a blue shift in the PL peak.

The Raman spectra of the same nanowires and $In_{0.53}Ga_{0.47}As$ 2D layer are shown in Figure 4b. The Raman spectrum of InGaAs contains four peaks resulting from incident laser photon interactions with the four transverse and longitudinal optical phonons (TO and LO), TO_{GaAs}, TO_{InAs}, LO_{GaAs}, and LO_{InAs}. While the TO−phonon interactions are generally weak, the LO_{GaAs} interaction will dominate even in indium-rich InGaAs. Therefore, the LO_{GaAs} peak can be used as a marker of composition.[27] We observe a shift of the nanowire LO_{GaAs} peak by approximately 10 cm^{-1} as compared with the 2D layer. Both the strain %, *s*, and indium fraction, *x*, in $In_xGa_{1-x}As$ will shift the LO_{GaAs} peak position and the position of the PL peak maxima.[26−29] By using a combined model of how *s* and *x* determine the peak position in both PL and Raman, *s* and *x* can be calculated (details are found in Supporting Information). Using this method, we find that the nanowires are $In_{0.78\pm0.03}Ga_{0.25\pm0.03}As$ with 0.77 ± 0.15% compressive strain if the regrown film is $In_{0.53}Ga_{0.47}As$. For the sample with nominal $In_{0.63}Ga_{0.37}As$ growth, we obtain $In_{0.85\pm0.03}Ga_{0.15\pm0.03}As$ with 1 ± 0.15% compressive strain for the nanowires. The composition shift of the nanowires may be explained by a local change of growth kinetics and diffusion, such as precursor flows, due to the HSQ mask. The expected strain in 2D layers of such compositions is 1.75 and 2.2%, respectively, indicating a partial strain relaxation mechanism in the nanowires.[26]

CONCLUSION

We have fabricated MOSFET devices to characterize the electron transport properties of selectively grown $In_{0.85}Ga_{0.15}As$ nanowires. The nanowires exhibit μ_e = 3300 ± 300 $cm^2/V\cdot s$, among the highest reported values for nanowires of similar dimensions. We also optically characterized our nanowires and found an unintentional increase of indium in the composition as well as partial strain relaxation. These results highlight the potential use of selectively regrown nanowires as the channel in high-performance electrical devices.

Conflict of Interest: The authors declare no competing financial interest.

Supporting Information Available: The Supporting Information is available free of charge on the ACS Publications website at DOI: 10.1021/acsnano.5b03318.

Additional information, figures, and optical characterization (PDF)

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